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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,454	09/22/2003	Ta-Chung Wu	17620R-002600US	2352

20350 7590 05/11/2004

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EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 05/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/668,454	TA-CHUNG WU	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *092203* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-4, 6, 9, and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Bhakta et al. (U.S. Pub. 2002/0081817).

In re claim 1, **Bhakta** discloses a method of forming a bottom oxide layer in a trench structure, the method comprising: (a) providing a semiconductor substrate **(FIGS. 3a-i: 10)** and forming a trench structure **(FIG. 3f: 18)** on said semiconductor substrate (page 2, paragraphs [0015]-[0019]); (b) performing a the plasma-enhanced chemical vapor deposition (PECVD) process with tetraethylorthosilicate (TEOS) as a gas source to deposit an oxide layer **(FIG. 3h: 22)** on the bottom and sidewall of the trench structure and the semiconductor substrate (page 2, paragraphs [0020]-[0021]); and (c) removing the oxide layer on the sidewall of the trench structure substantially completely and the oxide layer on the bottom of said trench structure partially to define a remaining oxide layer as the bottom oxide layer (pages 2-3, paragraphs [0024]-[0026] and **FIGS. 3j-l**).

In re claim 2, **Bhakta** discloses wherein the step (a) further comprises: (a1) forming a pad oxide layer **(FIGS. 3d-j: 12)** on the semiconductor substrate **(FIGS. 3a-l: 10)**; (a2) forming a silicon nitride layer **(FIGS. 3d-j: 14)** on said pad oxide layer; and

(a3) removing the silicon nitride layer, the pad oxide layer and the semiconductor substrate partially to form the trench structure **(FIG. 3f: 18)** (page 2, paragraphs [0017]-[0018]).

In re claim 3, **Bhakta** discloses wherein the step (a3) is performed by a photolithography and dry-etching process (page 2, paragraph [0018]).

In re claim 4, **Bhakta** discloses wherein the trench structure has an aspect ratio between about 3.0 and about 4.0 (page 2, paragraph [0018] and **FIG. 3f**).

In re claim 6, **Bhakta** discloses wherein a ratio of a thickness of the oxide layer deposited on the bottom of the trench structure to a thickness of the oxide layer deposited on the sidewall of the trench structure is between about 1.5 and about 2.3 (page 2, paragraph [0019] and **FIG. 3h**).

In re claim 9, **Bhakta** discloses wherein after the step (c), the steps of depositing and removing the oxide layer are repeated in sequence for allowing the bottom oxide layer to reach a required thickness **(FIGS. 3h-l)**.

In re claim 10, **Bhakta** discloses wherein the oxide layer comprises a silicon oxide layer (page 2, paragraph [0020]).

2. Claims 11-14, 16 and 19-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Bhakta et al. (U.S. Pub. 2002/0081817).

In re claim 11, **Bhakta** discloses a method of fabricating a trench-type power MOSFET, the method comprising: (a) providing a semiconductor substrate **(FIGS. 3a-i: 10)** and forming a trench structure **(FIG. 3f: 18)** on said semiconductor substrate (page 2, paragraphs [0015]-[0019]); (b) performing the plasma-enhanced chemical vapor

deposition (PECVD) process with tetraethylorthosilicate (TEOS) as a gas source to deposit an oxide layer **(FIG. 3h: 22)** on the bottom and sidewall of the trench structure and the semiconductor substrate (page 2, paragraphs [0020]-[0021]); (c) removing the oxide layer on the sidewall of the trench structure substantially completely and the oxide layer on the bottom of said trench structure partially to define a remaining oxide layer as the bottom oxide layer (pages 2-3, paragraphs [0024]-[0026] and **FIGS. 3j-l**); and forming the trench-type power MOSFET device in the trench structure (page 1, paragraph [0002] and page 3, paragraph [0028]).

In re claim 12, **Bhakta** discloses wherein the step (a) further comprises: (a1) forming a pad oxide layer **(FIGS. 3d-j: 12)** on the semiconductor substrate **(FIGS. 3a-l: 10)**; (a2) forming a silicon nitride layer **(FIGS. 3d-j: 14)** on said pad oxide layer; and (a3) removing the silicon nitride layer, the pad oxide layer and the semiconductor substrate partially to form the trench structure **(FIG. 3f: 18)** (page 2, paragraphs [0017]-[0018]).

In re claim 13, **Bhakta** discloses wherein the step (a3) is performed by a photolithography and dry-etching process (page 2, paragraph [0018]).

In re claim 14, **Bhakta** discloses wherein the trench structure has an aspect ratio between about 3.0 and about 4.0 (page 2, paragraph [0018] and **FIG. 3f**).

In re claim 16, **Bhakta** discloses wherein a ratio of a thickness of the oxide layer deposited on the bottom of the trench structure to a thickness of the oxide layer deposited on the sidewall of the trench structure is between about 1.5 and about 2.3 (page 2, paragraph [0019] and **FIG. 3h**).

In re claim 19, **Bhakta** discloses wherein after the step (c), the steps of depositing and removing the oxide layer are repeated in sequence for allowing the bottom oxide layer to reach a required thickness **(FIGS. 3h-l)**.

In re claim 20, **Bhakta** discloses wherein the oxide layer comprises a silicon oxide layer (page 2, paragraph [0020]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 5, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhakta et al. (U.S. Pub. 2002/0081817) in view of Ahn (U.S. Patent 6,596,607).

In re claim 5, **Bhakta** discloses wherein the plasma-enhanced chemical vapor deposition (PECVD) process is performed at a temperature of about 600°C to about 650°C (page 2, paragraphs [0020]-[0021]) but does not explicitly disclose the temperature ranges as recited by the Applicants. However, there is no evidence indicating the temperature range is critical and it has been held that it is not inventive to discover the optimum or workable range of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant

must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

In re claim 7, **Bhakta** does not explicitly disclose wherein the step (c) is performed by a wet-etching process.

Ahn discloses a method of forming a bottom oxide layer in a trench structure, the method comprising: (a) providing a semiconductor substrate **(FIG. 5: 100)** and forming a trench structure **(FIG. 5: 121)** on said semiconductor substrate (col. 4, lines 3-12); (b) performing a the plasma-enhanced chemical vapor deposition (PECVD) process with tetraethylorthosilicate (TEOS) as a gas source to deposit an oxide layer **(FIG. 6: 119)** on the bottom and sidewall of the trench structure and the semiconductor substrate (col. 4, lines 21-32); and (c) removing the oxide layer on the sidewall of the trench structure substantially completely and the oxide layer on the bottom of said trench structure partially to define a remaining oxide layer **(FIG. 7: 129)** as the bottom oxide layer by a wet-etching process (col. 4, lines 33-48). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Bhakta and Ahn to enable the wet-etching process to remove the oxide layer of Bhakta to be performed and furthermore because at this stage, an anisotropic etching may cause damage to the sidewall of the trench, therefore a wet etching process is advantageous (col. 4, lines 36-39).

In re claim 8, **Ahn** discloses wherein an etching selectivity of oxide layer on the sidewall of the trench structure to the oxide layer on the bottom of the trench structure is between about 2.5 and about 3 (col. 4, lines 33-48 and **FIGS. 5-8**).

4. Claims 15, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhakta et al. (U.S. Pub. 2002/0081817) in view of Ahn (U.S. Patent 6,596,607).

In re claim 15, **Bhakta** discloses wherein the plasma-enhanced chemical vapor deposition (PECVD) process is performed at a temperature of about 600°C to about 650°C (page 2, paragraphs [0020]-[0021]) but does not explicitly disclose the temperature ranges as recited by the Applicants. However, there is no evidence indicating the temperature range is critical and it has been held that it is not inventive to discover the optimum or workable range of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05.

In re claim 17, **Bhakta** does not explicitly disclose wherein the step (c) is performed by a wet-etching process.

Ahn discloses a method of forming a bottom oxide layer in a trench structure, the method comprising: (a) providing a semiconductor substrate **(FIG. 5: 100)** and forming a trench structure **(FIG. 5: 121)** on said semiconductor substrate (col. 4, lines 3-12); (b) performing a the plasma-enhanced chemical vapor deposition (PECVD) process with tetraethylorthosilicate (TEOS) as a gas source to deposit an oxide layer **(FIG. 6: 119)** on the bottom and sidewall of the trench structure and the semiconductor substrate (col. 4, lines 21-32); and (c) removing the oxide layer on the sidewall of the trench structure substantially completely and the oxide layer on the bottom of said trench structure partially to define a remaining oxide layer **(FIG. 7: 129)** as the bottom oxide layer by a wet-etching process (col. 4, lines 33-48). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Bhakta and

Ahn to enable the wet-etching process to remove the oxide layer of Bhakta to be performed and furthermore because at this stage, an anisotropic etching may cause damage to the sidewall of the trench, therefore a wet etching process is advantageous (col. 4, lines 36-39).

In re claim 18, **Ahn** discloses wherein an etching selectivity of oxide layer on the sidewall of the trench structure to the oxide layer on the bottom of the trench structure is between about 2.5 and about 3 (col. 4, lines 33-48 and **FIGS. 5-8**).

5. Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhakta et al. (U.S. Pub. 2002/0081817) in view of Ahn (U.S. Patent 6,596,607).

In re claim 21, **Bhakta** discloses a method of forming a bottom oxide layer in a trench structure, the method comprising: (a) providing a substrate **(FIGS. 3a-i: 10)** including a trench **(FIG. 3f: 18)** having a bottom and a sidewall (page 2, paragraphs [0015]-[0019]); (b) depositing an oxide layer **(FIG. 3h: 22)** on the bottom and sidewall of the trench by plasma-enhanced chemical vapor deposition (PECVD) process with tetraethylorthosilicate (TEOS) as a gas source (page 2, paragraphs [0020]-[0021]); and (c) removing the oxide layer on the sidewall of the trench structure substantially completely and the oxide layer on the bottom of said trench structure partially to form a remaining oxide layer as the bottom oxide layer on the bottom of the trench (pages 2-3, paragraphs [0024]-[0026] and **FIGS. 3j-l**).

Bhakta discloses wherein the plasma-enhanced chemical vapor deposition (PECVD) process is performed at a temperature of about 600°C to about 650°C (page 2, paragraphs [0020]-[0021]) but does not explicitly disclose the temperature ranges as

recited by the Applicants. However, there is no evidence indicating the temperature range is critical and it has been held that it is not inventive to discover the optimum or workable range of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05.

In re claim 22, **Bhakta** does not explicitly disclose wherein the step the oxide layer is removed by a wet-etching process having a higher etching selectivity of the oxide layer on the sidewall of the trench to the oxide layer on the bottom of the trench.

Ahn discloses a method of forming a bottom oxide layer in a trench structure, the method comprising: (a) providing a semiconductor substrate **(FIG. 5: 100)** and forming a trench structure **(FIG. 5: 121)** on said semiconductor substrate (col. 4, lines 3-12); (b) performing a the plasma-enhanced chemical vapor deposition (PECVD) process with tetraethylorthosilicate (TEOS) as a gas source to deposit an oxide layer **(FIG. 6: 119)** on the bottom and sidewall of the trench structure and the semiconductor substrate (col. 4, lines 21-32); and (c) removing the oxide layer on the sidewall of the trench structure substantially completely and the oxide layer on the bottom of said trench structure partially to define a remaining oxide layer **(FIG. 7: 129)** as the bottom oxide layer by a wet-etching process having a higher etching selectivity of the oxide layer on the sidewall of the trench to the oxide layer on the bottom of the trench (col. 4, lines 33-48). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Bhakta and Ahn to enable the wet-etching process to remove the oxide layer of Bhakta to be performed and furthermore because at this stage, an

anisotropic etching may cause damage to the sidewall of the trench, therefore a wet etching process is advantageous (col. 4, lines 36-39).

In re claim 23, **Ahn** discloses wherein an etching selectivity of oxide layer on the sidewall of the trench structure to the oxide layer on the bottom of the trench structure is between about 2.5 and about 3 (col. 4, lines 33-48 and **FIGS. 5-8**).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Primary Examiner
Khiem Minh Le
5/7/2004

K.N.
May 7, 2004